National Semiconductor

September 2007

LMH6552
1.5 GHz Fully Differential Amplifier

General Description

The LMH6552 is a high performance fully differential amplifier designed to provide the exceptional signal fidelity and wide large-signal bandwidth necessary for driving 8 to 14 bit high speed data acquisition systems. Using National's proprietary differential current mode input stage architecture, the LMH6552 allows operation at gains greater than unity without sacrificing response flatness, bandwidth, harmonic distortion, or output noise performance.

With external gain set resistors and integrated common mode feedback, the LMH6552 can be configured as either a differential input to differential output or single ended input to differential output gain block. The LMH6552 can be AC or DC coupled at the input which makes it suitable for a wide range of applications including communication systems and high speed oscilloscope front ends. The performance of the LMH6552 driving an ADC14DS105 is 86 dBc SFDR and 74 dBc SNR up to 40 MHz.

The LMH6552 is available in an 8-pin SOIC package as well as a space saving, thermally enhanced 8-Pin LLP package for higher performance.

Features

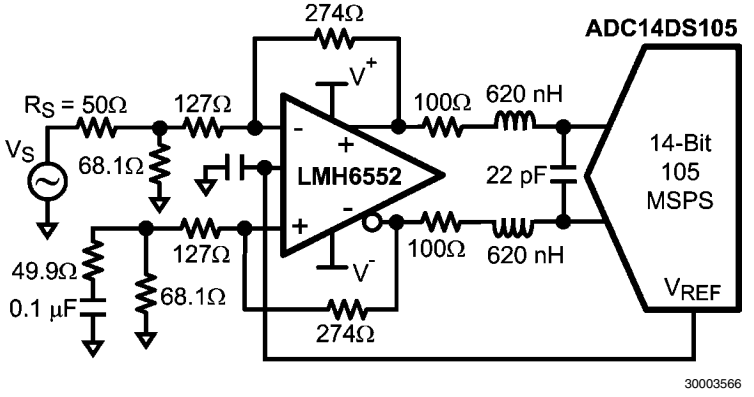
- 1.5 GHz –3 dB small signal bandwidth @ $A_V = 1$
- 1.25 GHz –3 dB large signal bandwidth @ $A_V = 1$
- 800 MHz bandwidth @ $A_V = 4$
- 450 MHz 0.1 dB flatness
- 3800 V/µs slew rate
- 10 ns settling time to 0.1%
- –90 dB THD @ 20 MHz
- –74 dB THD @ 70 MHz
- 20 ns enable/shutdown pin
- 5 to 12V operation

Applications

- Differential ADC driver
- Video over twisted pair
- Differential line driver
- Single end to differential converter
- High speed differential signaling
- IF/RF amplifier
- Level shift amplifier
- SAW filter buffer/driver

Typical Application

Single-Ended Input Differential Output ADC Driver



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 5)	
Human Body Model	2000V
Machine Model	200V
Supply Voltage	13.2V
Common Mode Input Voltage	$\pm V_S$
Maximum Input Current (pins 1, 2, 7, 8)	30 mA
Maximum Output Current (pins 4, 5)	(Note 4)
Soldering Information	
Infrared or Convection (20 sec)	235°C
Wave Soldering (10 sec)	260°C

Operating Ratings (Note 1)

Operating Temperature Range (Note 3)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Total Supply Voltage	4.5V to 12V
Package Thermal Resistance (θ_{JA})	
8-Pin SOIC	150°C/W
8-Pin LLP	58°C/W

±5V Electrical Characteristics (Note 2)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V^+ = +5V, V^- = −5V, A_V= 1, V_{CM} = 0V, $R_F = R_G$ = 357Ω, R_L = 500Ω, for single ended in, differential out. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
AC Performance (Differential)						
SSBW	Small Signal −3 dB Bandwidth (Note 8)	V_{OUT} = 0.2 V_{PP}, A_V = 1, R_L = 1 kΩ		1500		MHz
		V_{OUT} = 0.2 V_{PP}, A_V = 1		1000		
		V_{OUT} = 0.2 V_{PP}, A_V = 2		930		
		V_{OUT} = 0.2 V_{PP}, A_V = 4		810		
		V_{OUT} = 0.2 V_{PP}, A_V = 8		590		
LSBW	Large Signal −3 dB Bandwidth	V_{OUT} = 2 V_{PP}, A_V = 1, R_L = 1 kΩ		1250		MHz
		V_{OUT} = 2 V_{PP}, A_V = 1		950		
		V_{OUT} = 2 V_{PP}, A_V = 2		820		
		V_{OUT} = 2 V_{PP}, A_V = 4		740		
		V_{OUT} = 2 V_{PP}, A_V = 8		590		
	0.1 dB Bandwidth	V_{OUT} = 0.2 V_{PP}, A_V = 1		450		MHz
	Slew Rate	4V Step, A_V = 1		3800		V/µs
	Rise/Fall Time, 10%-90%	2V Step		600		ps
	0.1% Settling Time	2V Step		10		ns
	Overdrive Recovery Time	V_{IN} = 1.8V to 0V Step, A_V = 5 V/V		6		ns
Distortion and Noise Response						
HD2	2nd Harmonic Distortion	V_{OUT} = 2 V_{PP}, f = 20 MHz, R_L = 800Ω		−92		dBc
		V_{OUT} = 2 V_{PP}, f = 70 MHz, R_L = 800Ω		−74		
HD3	3rd Harmonic Distortion	V_{OUT} = 2 V_{PP}, f = 20 MHz, R_L = 800Ω		−93		dBc
		V_{OUT} = 2 V_{PP}, f = 70 MHz, R_L = 800Ω		−84		
IMD3	Two-Tone Intermodulation	f >70 MHz, Third Order Products, V_{OUT} = 2 V_{PP} Composite		−87		dBc
	Input Noise Voltage	f ≥ 1 MHz		1.1		$nV/\sqrt{Hz}$
	Input Noise Current	f ≥ 1 MHz		19.5		$pA/\sqrt{Hz}$
	Noise Figure (See *Figure 5*)	50Ω System, A_V = 9, 10 MHz		10.3		dB
Input Characteristics						
I_{BI}	Input Bias Current (Note 10)			60	110	µA
$I_{Boffset}$	Input Bias Current Differential (Note 7)	V_{CM} = 0V, V_{ID} = 0V, $I_{Boffset} = (I_{B-} - I_{B+})/2$		2.5	18	µA
CMRR	Common Mode Rejection Ratio (Note 7)	DC, V_{CM} = 0V, V_{ID} = 0V		80		dBc
R_{IN}	Input Resistance	Differential		15		Ω

Symbol	Parameter	Conditions	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
C_{IN}	Input Capacitance	Differential		0.5		pF
CMVR	Input Common Mode Voltage Range	CMRR > 38 dB	±3.5	±3.8		V
Output Performance						
	Output Voltage Swing (Note 7)	Differential Output	14.8	15.4		V_{PP}
I_{OUT}	Linear Output Current (Note 7)	V_{OUT} = 0V	±70	±80		mA
I_{SC}	Short Circuit Current	One Output Shorted to Ground V_{IN} = 2V Single Ended (Note 6)		±141		mA
	Output Balance Error	ΔV_{OUT} Common Mode /ΔV_{OUT} Differential , ΔV_{OD} = 1V, f < 1 MHz		−60		dB
Miscellaneous Performance						
Z_T	Open Loop Transimpedance	Differential		108		dBΩ
PSRR	Power Supply Rejection Ratio	DC, ΔV_S = ±1V		80		dB
I_S	Supply Current (Note 7)	R_L = ∞	19	22.5	25 **28**	mA
	Enable Voltage Threshold		3.0			V
	Disable Voltage Threshold				2.0	V
	Enable/Disable time			15		ns
I_{SD}	Disable Shutdown Current			500	600	µA
Output Common Mode Control Circuit						
	Common Mode Small Signal Bandwidth	V_{IN+} = V_{IN-} = 0		400		MHz
	Slew Rate	V_{IN+} = V_{IN-} = 0		607		V/µs
V_{OSCM}	Input Offset Voltage	Common Mode, V_{ID} = 0, V_{CM} = 0		1.5	±16.5	mV
	Input Bias Current	(Note 9)		−3.2	±8	µA
	Voltage Range		±3.7	±3.8		V
	CMRR	Measure V_{OD}, V_{ID} = 0V		80		dB
	Input Resistance			200		kΩ
	Gain	$\Delta V_{O,CM}/\Delta V_{CM}$	0.995	1.0	1.012	V/V

±2.5V Electrical Characteristics (Note 2)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V^+ = +2.5V, V^- = −2.5V, A_V = 1, V_{CM} = 0V, R_F = R_G = 357Ω, R_L = 500Ω, for single ended in, differential out. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
SSBW	Small Signal −3 dB Bandwidth (Note 8)	V_{OUT} = 0.2 V_{PP}, A_V = 1, R_L = 1 kΩ		1100		MHz
		V_{OUT} = 0.2 V_{PP}, A_V = 1		800		
		V_{OUT} = 0.2 V_{PP}, A_V = 2		740		
		V_{OUT} = 0.2 V_{PP}, A_V = 4		660		
		V_{OUT} = 0.2 V_{PP}, A_V = 8		498		
LSBW	Large Signal −3 dB Bandwidth	V_{OUT} = 2 V_{PP}, A_V = 1, R_L = 1 kΩ		820		MHz
		V_{OUT} = 2 V_{PP}, A_V = 1		690		
		V_{OUT} = 2 V_{PP}, A_V = 2		620		
		V_{OUT} = 2 V_{PP}, A_V = 4		589		
		V_{OUT} = 2 V_{PP}, A_V = 8		480		
	0.1 dB Bandwidth	V_{OUT} = 0.2 V_{PP}, A_V = 1		300		MHz
	Slew Rate	2V Step, A_V = 1		2100		V/µs
	Rise/Fall Time, 10% to 90%	2V Step		700		ps

Symbol	Parameter	Conditions	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
	0.1% Settling Time	2V Step		10		ns
	Overdrive Recovery Time	V_{IN} = 0.7 V to 0 V Step, A_V = 5 V/V		6		ns
Distortion and Noise Response						
HD2	2nd Harmonic Distortion	V_{OUT} = 2 V_{PP}, f = 20 MHz, R_L = 800Ω		82		dBc
		V_{OUT} = 2 V_{PP}, f = 70 MHz, R_L = 800Ω		65		
HD3	3rd Harmonic Distortion	V_{OUT} = 2 V_{PP}, f = 20 MHz, R_L = 800Ω		79		dBc
		V_{OUT} = 2 V_{PP}, f = 70 MHz, R_L = 800Ω		67		
IMD3	Two-Tone Intermodulation	f ≥ 70 MHz, Third Order Products, V_{OUT} = 2 V_{PP} Composite		−77		dBc
	Input Noise Voltage	f ≥ 1 MHz		1.1		$nV/\sqrt{Hz}$
	Input Noise Current	f ≥ 1 MHz		19.5		$pA/\sqrt{Hz}$
	Noise Figure (See *Figure 5*)	50Ω System, A_V = 9, 10 MHz		10.2		dB
Input Characteristics						
I_{BI}	Input Bias Current (Note 10)			54	90	µA
$I_{Boffset}$	Input Bias Current Differential (Note 7)	V_{CM} = 0V, V_{ID} = 0V, $I_{Boffset}$ = (I_{B^-} - I_{B^+})/2		2.3	18	µA
CMRR	Common-Mode Rejection Ratio (Note 7)	DC, V_{CM} = 0V, V_{ID} = 0V		75		dBc
R_{IN}	Input Resistance	Differential		15		Ω
C_{IN}	Input Capacitance	Differential		0.5		pF
CMVR	Input Common Mode Range	CMRR > 38 dB	±1.0	±1.3		V
Output Performance						
	Output Voltage Swing (Note 7)	Differential Output	5.6	6.0		V_{PP}
I_{OUT}	Linear Output Current (Note 7)	V_{OUT} = 0V	±55	±65		mA
I_{SC}	Short Circuit Current	One Output Shorted to Ground, V_{IN} = 2V Single Ended (Note 6)		±131		mA
	Output Balance Error	ΔV_{OUT} Common Mode /ΔV_{OUT} Differential , ΔV_{OD} = 1V, f < 1 MHz		60		dB
Miscellaneous Performance						
ZT	Open Loop Transimpedance	Differential		107		dBΩ
PSRR	Power Supply Rejection Ratio	DC, ΔV_S = ±1V		80		dB
I_S	Supply Current (Note 7)	R_L = ∞	17	20.4	24 **27**	mA
	Enable Voltage Threshold		3.0			V
	Disable Voltage Threshold				2.0	V
	Enable/Disable Time			15		ns
I_{SD}	Disable Shutdown Current			500	600	µA
Output Common Mode Control Circuit						
	Common Mode Small Signal Bandwidth	V_{IN+} = V_{IN-} = 0		310		MHz
	Slew Rate	V_{IN+} = V_{IN-} = 0		430		V/µs
V_{OSCM}	Input Offset Voltage	Common Mode, V_{ID} = 0, V_{CM} = 0		1.65	±15	mV
	Input Bias Current	(Note 9)		−2.9		µA
	Voltage Range		±1.19	±1.25		V
	CMRR	Measure V_{OD}, V_{ID} = 0V		80		dB
	Input Resistance			200		kΩ
	Gain	$\Delta V_{O,CM}/\Delta V_{CM}$	0.995	1.0	1.012	V/V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications, see the Electrical Characteristics tables.

Note 2: Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. See Applications Section for information on temperature de-rating of this device." Min/Max ratings are based on product characterization and simulation. Individual parameters are tested as noted.

Note 3: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Note 4: The maximum output current (I_{OUT}) is determined by device power dissipation limitations. See the Power Dissipation section of the Application Section for more details.

Note 5: Human Body Model, applicable std. MIL-STD-883, Method 30157. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC). Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

Note 6: Short circuit current should be limited in duration to no more than 10 seconds. See the Power Dissipation section of the Application Information for more details.

Note 7: Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

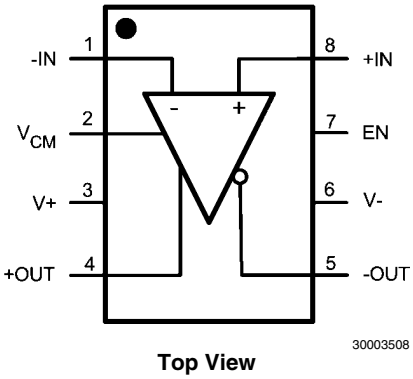
Note 8: Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.

Note 9: Negative input current implies current flowing out of the device.

Note 10: I_{BI} is referred to a differential output offset voltage by the following relationship: $V_{OD(offset)} = I_{BI}*2R_F$

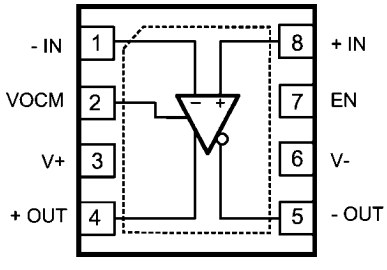
Connection Diagrams

8-Pin SOIC



Top View

8-Pin LLP



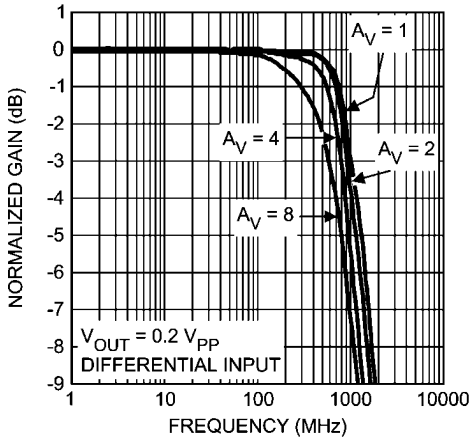
Top View

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
8-Pin SOIC	LMH6552MA	LMH6552MA	95/Rails	M08A
	LMH6552MAX		2.5k Units Tape and Reel	
8-Pin LLP	LMH6552SD	6552	1k Units Tape and Reel	SDA08C
	LMH6552SDX		4.5k Units Tape and Reel	

Typical Performance Characteristics $V^+ = +5V$, $V^- = -5V$ ($T_A = 25°C$, $R_F = R_G = 357\Omega$, $R_L = 500\Omega$, $A_V = 1$, for single ended in, differential out, unless specified).

Frequency Response vs. Gain



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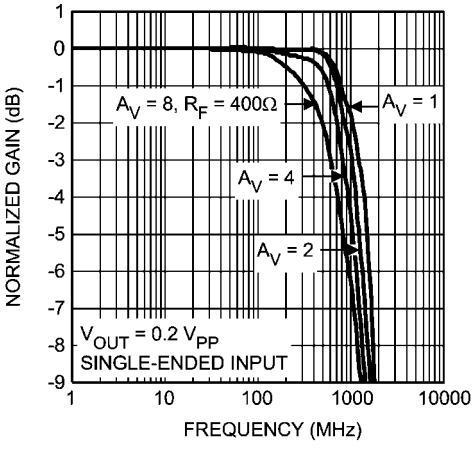
Frequency Response vs. Gain



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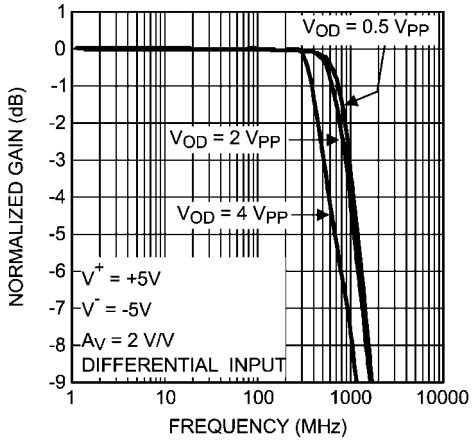
Frequency Response vs. V_{OUT}



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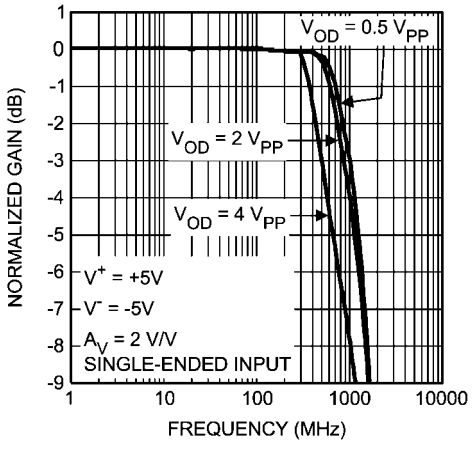
Frequency Response vs. V_{OUT}



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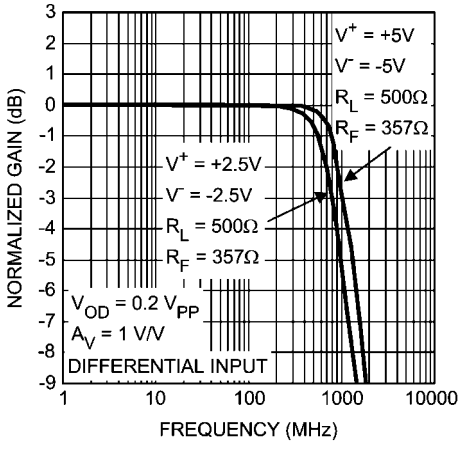
Frequency Response vs. Supply Voltage



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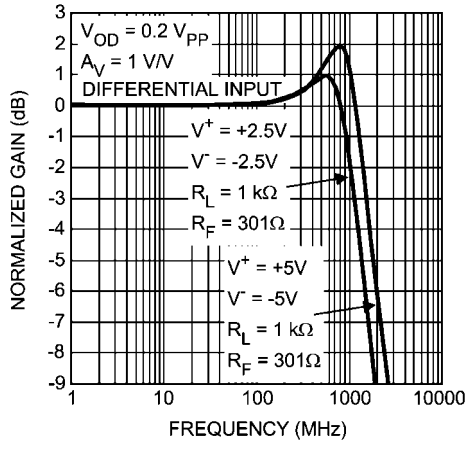
Frequency Response vs. Supply Voltage



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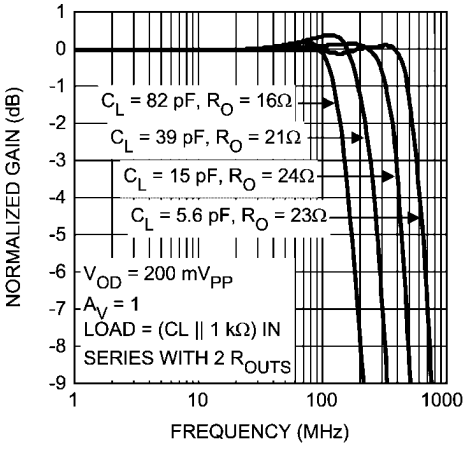
Frequency Response vs. Capacitive Load



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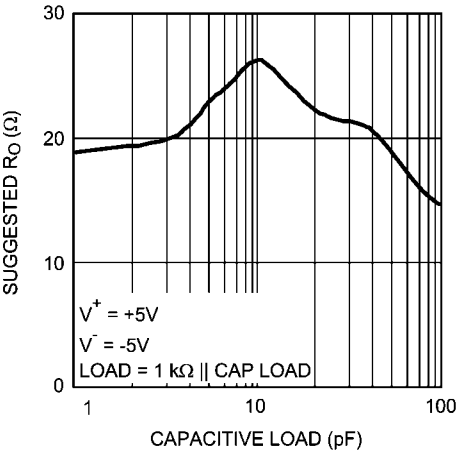
Suggested R_{OUT} vs. Capacitive Load



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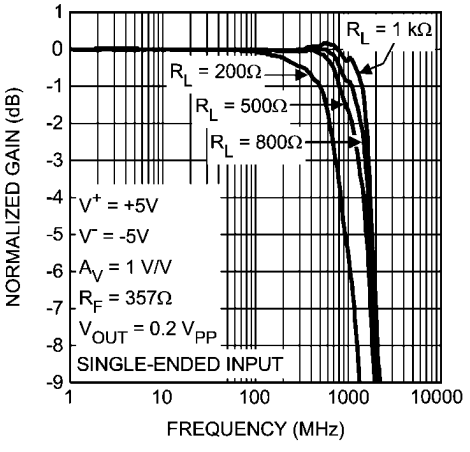
Frequency Response vs. Resistive Load



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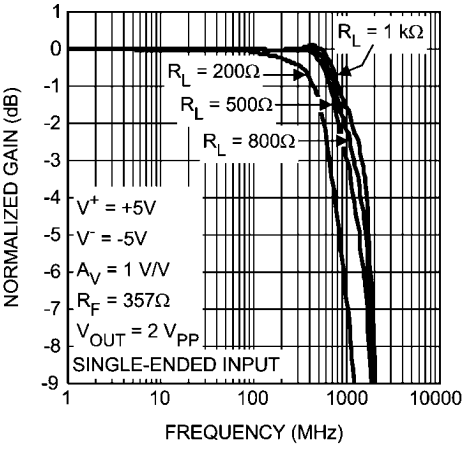
Frequency Response vs. Resistive Load



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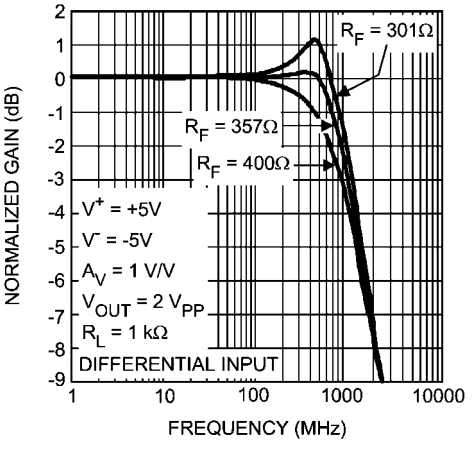
Frequency Response vs. R_F



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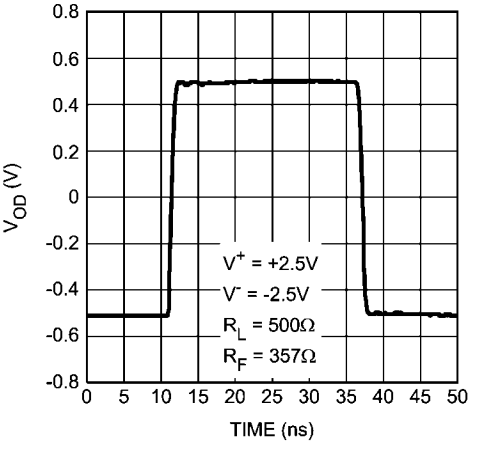
1 V_{PP} Pulse Response Single Ended Input



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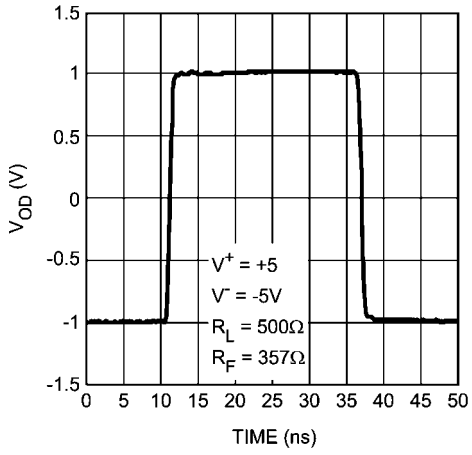
2 V_{PP} Pulse Response Single Ended Input



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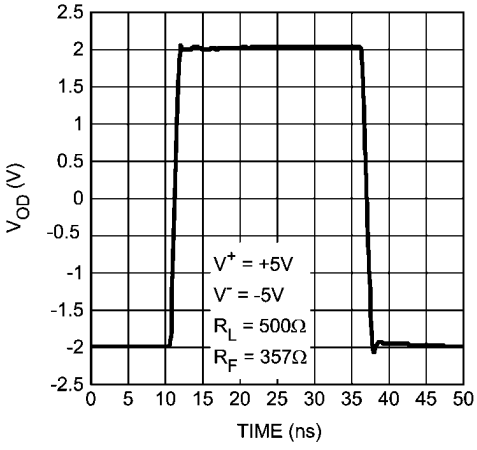
Large Signal Pulse Response



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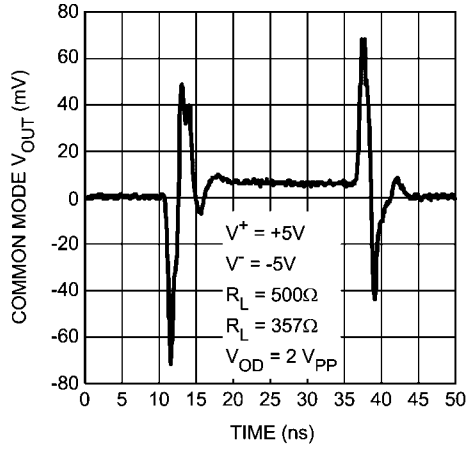
Output Common Mode Pulse Response



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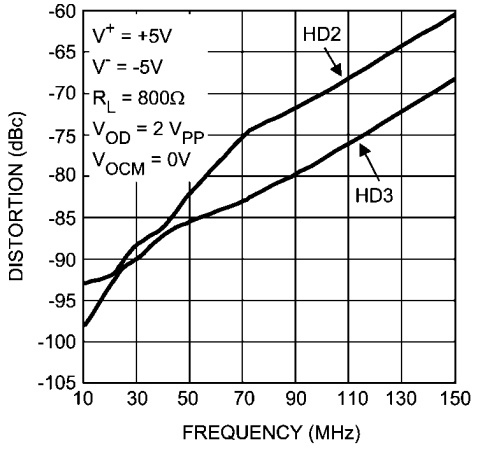
Distortion vs. Frequency Single Ended Input



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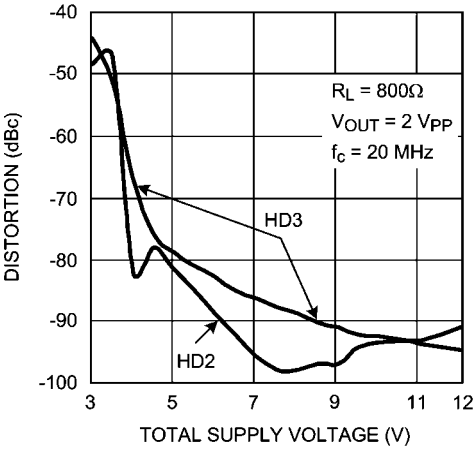
Distortion vs. Supply Voltage



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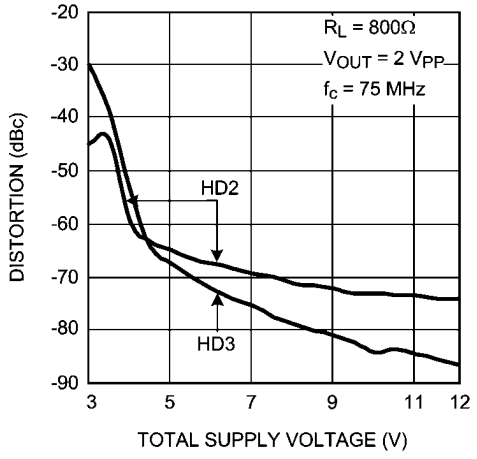
Distortion vs. Supply Voltage



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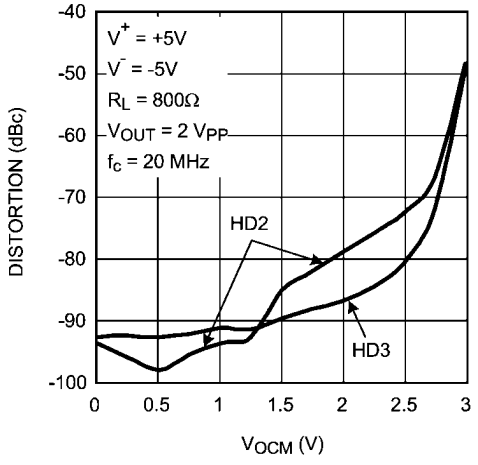
Distortion vs. Output Common Mode Voltage



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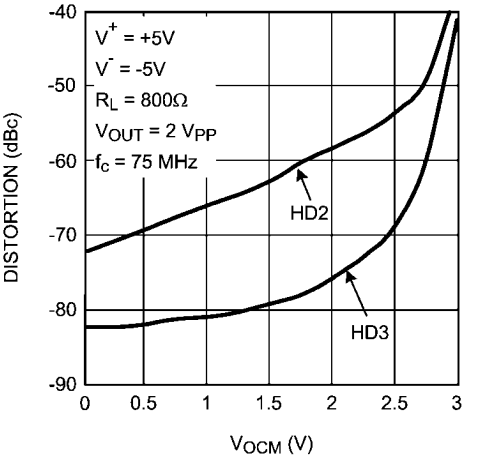
Distortion vs. Output Common Mode Voltage



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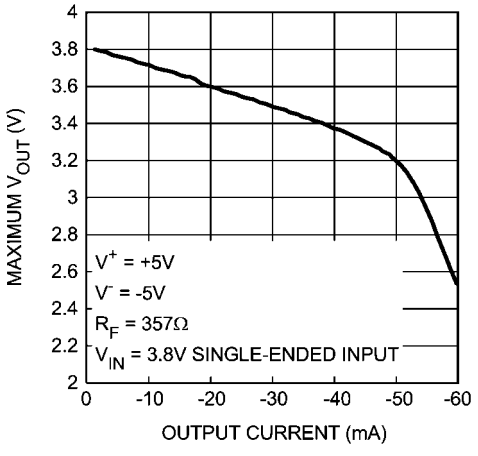
Maximum V_{OUT} vs. I_{OUT}



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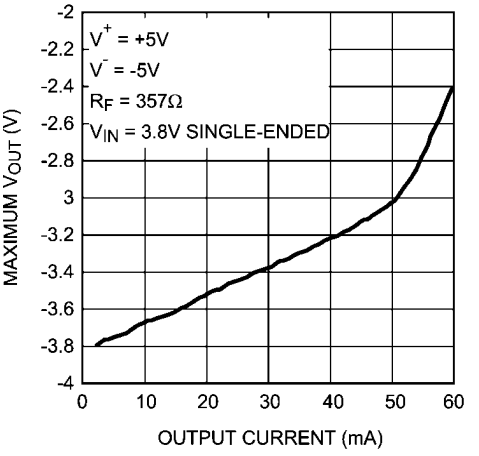
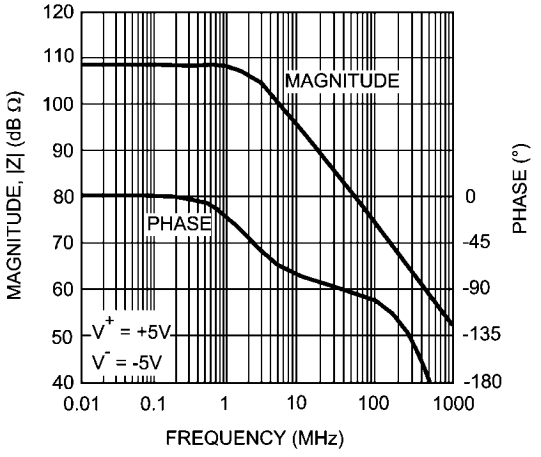
Minimum V_{OUT} vs. I_{OUT}



30003531

Open Loop Transimpedance



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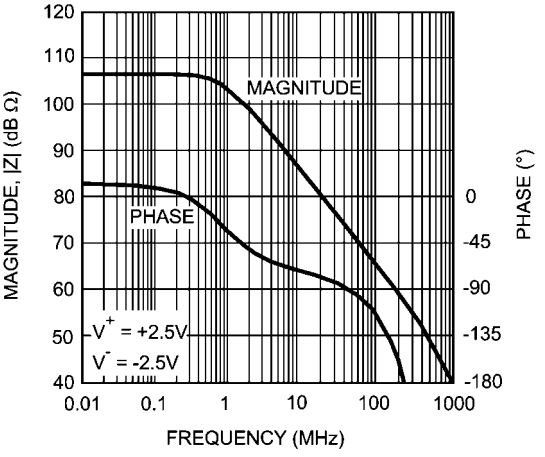
Open Loop Transimpedance



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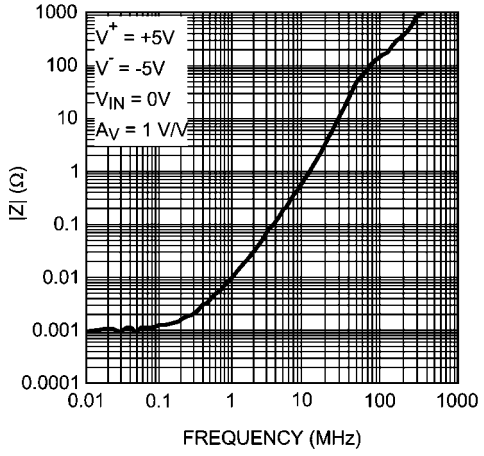
Closed Loop Output Impedance



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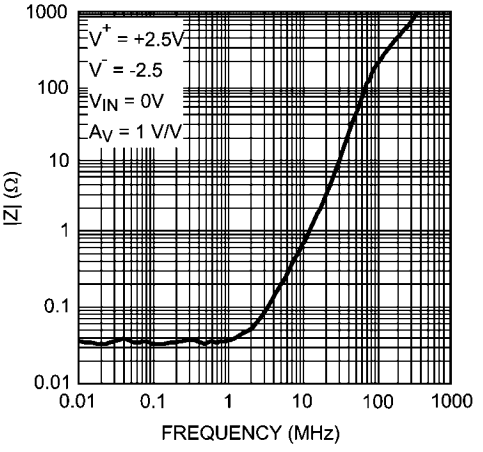
Closed Loop Output Impedance



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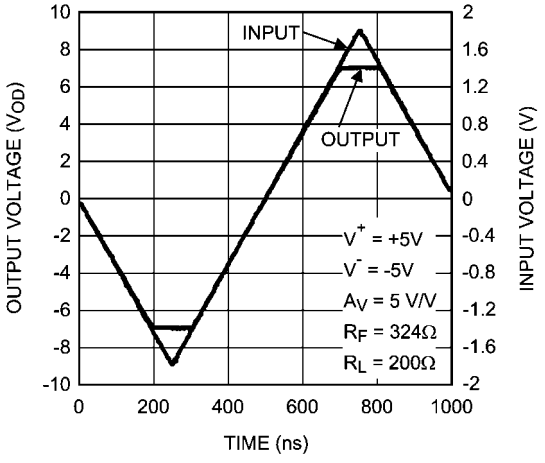
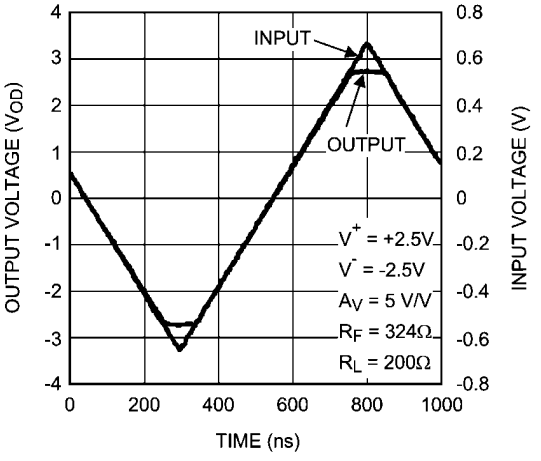
Overdrive Recovery



30003557

Overdrive Recovery



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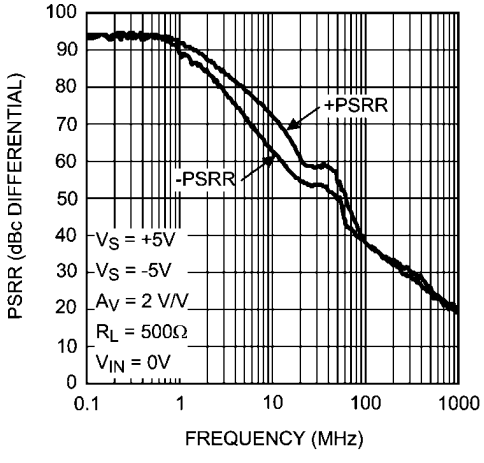
PSRR



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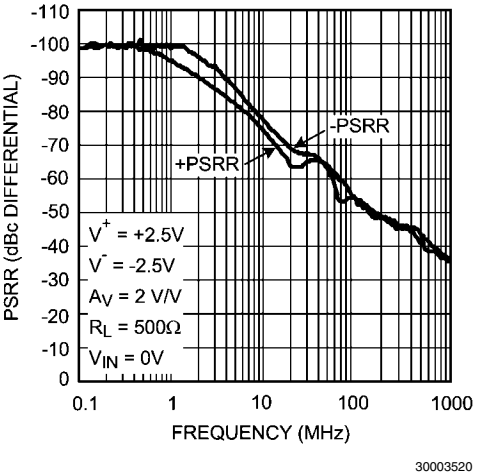
PSRR



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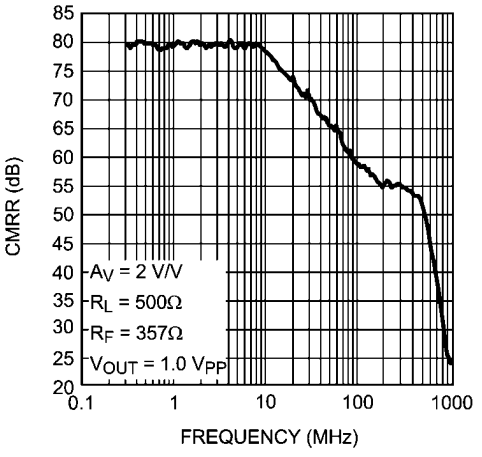
CMRR



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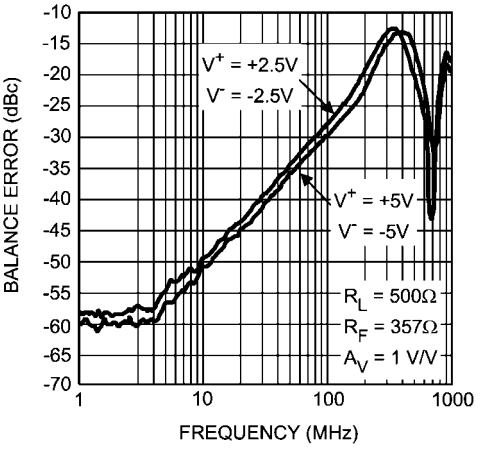
Balance Error



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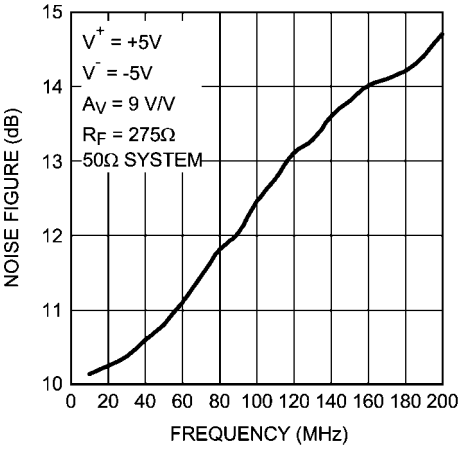
Noise Figure



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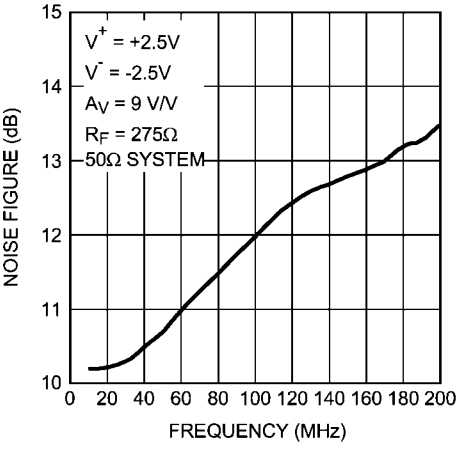
Noise Figure



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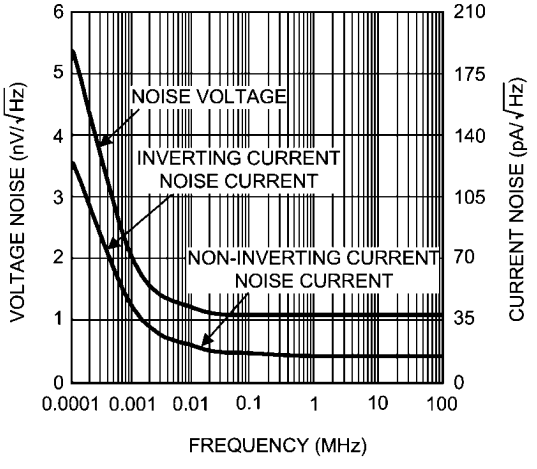
Input Noise vs. Frequency



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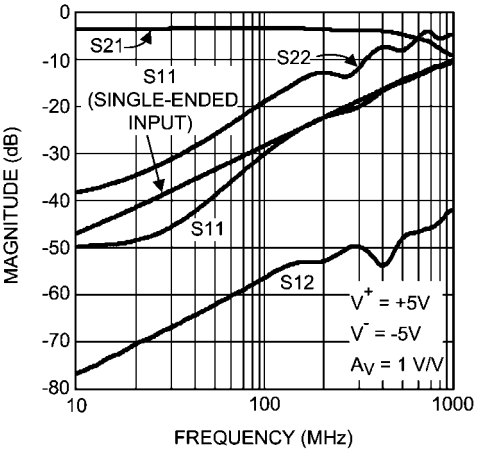
Differential S-Parameter Magnitude vs. Frequency



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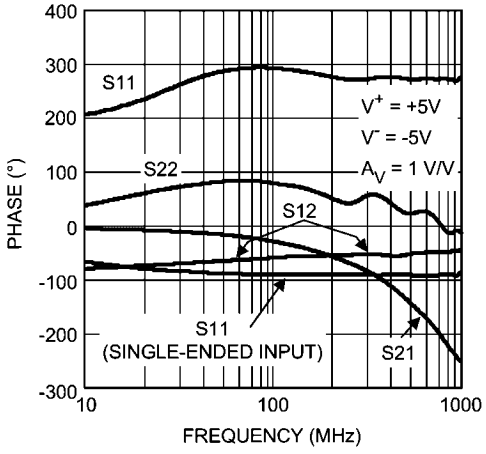
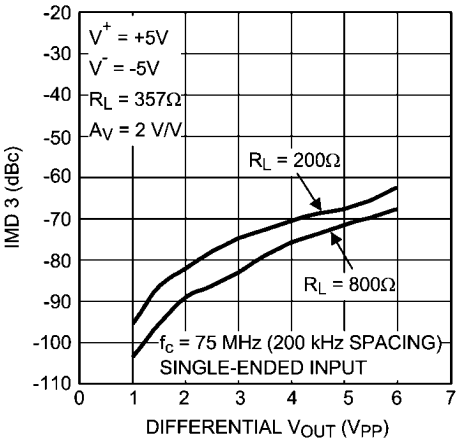
Differential S-Parameter Phase vs. Frequency



30003556

3rd Order Intermodulation Products vs. V_{OUT}



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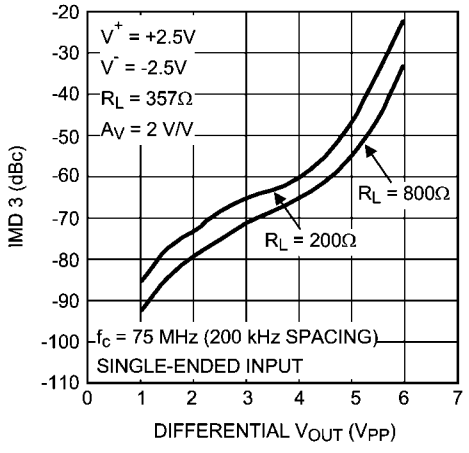
3rd Order Intermodulation Products vs. V_{OUT}



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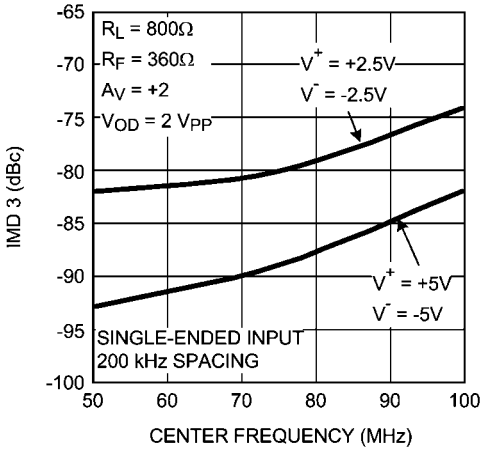
3rd Order Intermodulation Products vs. Center Frequency



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Application Information

The LMH6552 is a fully differential current feedback amplifier with integrated output common mode control, designed to provide low distortion amplification to wide bandwidth differential signals. The common mode feedback circuit sets the output common mode voltage independent of the input common mode, as well as forcing the V^+ and V^- outputs to be equal in magnitude and opposite in phase, even when only one of the inputs is driven as in single to differential conversion.

The proprietary current feedback architecture of the LMH6552 offers gain and bandwidth independence with exceptional gain flatness and noise performance, even at high values of gain, simply with the appropriate choice of R_{F1} and R_{F2}. Generally R_{F1} is set equal to R_{F2}, and R_{G1} equal to R_{G2}, so that the gain is set by the ratio R_F/R_G. Matching of these resistors greatly affects CMRR, DC offset error, and output balance. A minimum of 0.1% tolerance resistors are recommended for optimal performance, and the amplifier is internally compensated to operate with optimum gain flatness with values of R_F between 270Ω and 390Ω depending on package selection, PCB layout, and load resistance.

The output common mode voltage is set by the V_{CM} pin with a fixed gain of 1 V/V. This pin should be driven by a low impedance reference and should be bypassed to ground with a 0.1 µF ceramic capacitor. Any unwanted signal coupling into the V_{CM} pin will be passed along to the outputs, reducing the performance of the amplifier. This pin must not be left floating.

The LMH6552 can be operated on a supply range as either a single 5V supply or as a split +5V and −5V. Operation on a single 5V supply, depending on gain, is limited by the input common mode range; therefore, AC coupling may be required. For example, in a DC coupled input application on a single 5V supply, with a V_{CM} of 1.5V, the input common voltage at a gain of 1 will be 0.75V which is outside the minimum 1.2V to 3.8V input common mode range of the amplifier. The minimum V_{CM} for this application should be greater than 2.5V depending on output signal swing. Alternatively, AC coupling of the inputs in this example results in equal input and output common mode voltages, so a 1.5V V_{CM} would be achievable. Split supplies will allow much less restricted AC and DC coupled operation with optimum distortion performance.

The LMH6552 is equipped with an ENABLE pin to reduce power consumption when not in use. The ENABLE pin, when not driven, floats high (on). When the ENABLE pin is pulled low the amplifier is disabled and the amplifier output stage goes into a high impedance state so the feedback and gain set resistors determine the output impedance of the circuit. For this reason input to output isolation will be poor in the disabled state and the part is not recommended in multiplexed applications where outputs are all tied together.

LLP PACKAGE

Due to it's size and lower parasitics, the LLP requires the lower optimum value of 275Ω for R_F. This will give a flat frequency response with minimal peaking. With a lower R_F value the LLP package will have a reduction in noise compared to the SOIC with its optimum R_F = 360Ω.

FULLY DIFFERENTIAL OPERATION

The LMH6552 will perform best in a fully differential configuration. The circuit shown in *Figure 1* is a typical fully differential application circuit as might be used to drive an analog to digital converter (ADC). In this circuit the closed loop gain $A_V = V_{OUT}/ V_{IN} = R_F/R_G$, where the feedback is symmetric. The series output resistors, R_O, are optional and help keep the amplifier stable when presented with a capacitive load. Refer to the Driving Capacitive Loads section for details.

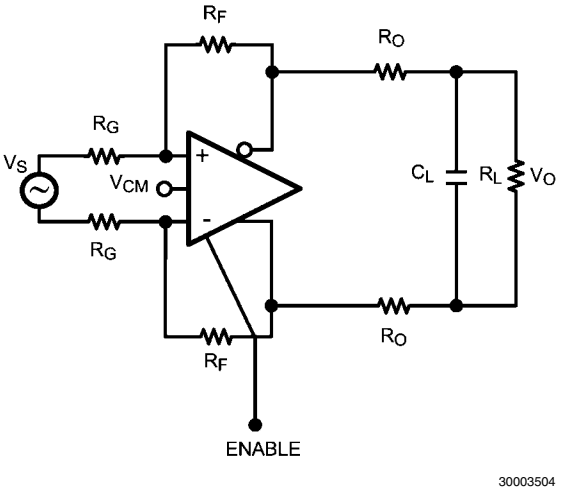


FIGURE 1. Typical Application

When driven from a differential source, the LMH6552 provides low distortion, excellent balance, and common mode rejection. This is true provided the resistors R_F, R_G and R_O are well matched and strict symmetry is observed in board layout. With an intrinsic device CMRR of 80 dB, using 0.1% resistors will give a worst case CMRR of around 60 dB for most circuits.

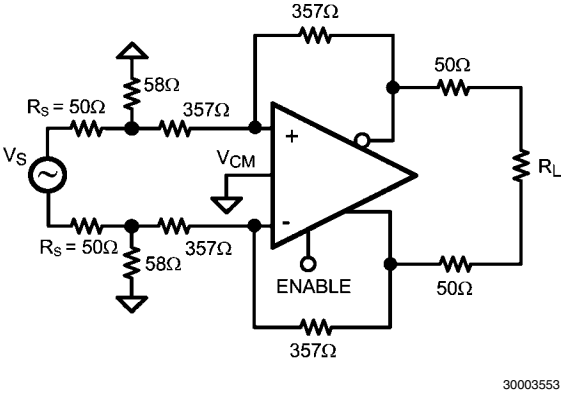


FIGURE 2. Differential S-Parameter Test Circuit

The circuit configuration shown in *Figure 2* was used to measure differential S parameters in a 50Ω environment at a gain of 1 V/V. Refer to the Differential S-Parameter vs. Frequency plots in the Typical Performance Characteristics section for measurement results.

SINGLE ENDED INPUT TO DIFFERENTIAL OUTPUT OPERATION

In many applications, it is required to drive a differential input ADC from a single ended source. Traditionally, transformers have been used to provide single to differential conversion, but these are inherently bandpass by nature and cannot be used for DC coupled applications. The LMH6552 provides excellent performance as a single-to-differential converter down to DC. *Figure 3* shows a typical application circuit where an LMH6552 is used to produce a differential signal from a single ended source.

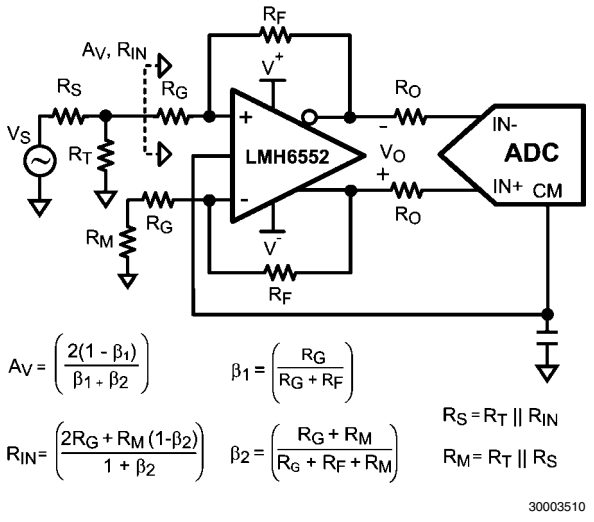


FIGURE 3. Single Ended Input with Differential Output

When using the LMH6552 in single-to-differential mode, the complimentary output is forced to a phase inverted replica of the driven output by the common mode feedback circuit as opposed to being driven by its own complimentary input. Consequently, as the driven input changes, the common mode feedback action results in a varying common mode voltage at the amplifier's inputs, proportional to the driving signal. Due to the non-ideal common mode rejection of the amplifier's input stage, a small common mode signal appears at the outputs which is superimposed on the differential output signal. The ratio of the change in output common mode voltage to output differential voltage is commonly referred to as output balance error. The output balance error response of the LMH6552 over frequency is shown in the Typical Performance Characteristics section.

To match the input impedance of the circuit in *Figure 3* to a specified source resistance, R_S, requires that $R_T \parallel R_{IN} = R_S$. The equations governing R_{IN} and A_V for single-to-differential operation are also provided in *Figure 3*. These equations, along with the source matching condition, must be solved iteratively to achieve the desired gain with the proper input termination. Component values for several common gain configurations in a 50Ω environment are given in Table 1.

Table 1. Gain Component Values for 50Ω System SOIC Package

Gain	R_F	R_G	R_T	R_M
0 dB	357Ω	348Ω	56.2Ω	26.4Ω
6 dB	357Ω	169Ω	61.8Ω	27.6Ω
12 dB	357Ω	76.8Ω	76.8Ω	30.9Ω

Table 2. Gain Component Values for 50Ω System LLP Package

Gain	R_F	R_G	R_T	R_M
0 dB	275Ω	255Ω	59Ω	26.7Ω
6 dB	275Ω	127Ω	68.1Ω	28.7Ω
12 dB	275Ω	54.9Ω	107Ω	34Ω

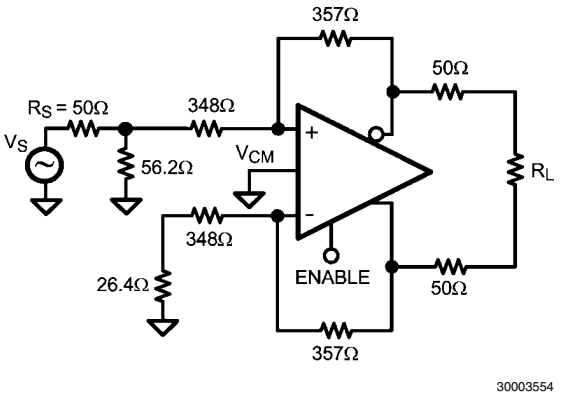


FIGURE 4. Single Ended Input S-Parameter Test Circuit (50Ω System)

The circuit shown in *Figure 4* was used to measure S-parameters for a single-to-differential configuration. The S-parameter plots in the Typical Performance Curves are taken using the recommended component values for 0 dB gain.

SINGLE SUPPLY OPERATION

Single supply operation is possible on supplies from 5V to 10V; however, as discussed earlier, AC input coupling is recommended for low supplies such as 5V due to input common mode limitations. An example of an AC coupled, single supply, single-to-differential circuit is shown in *Figure 5*. Note that when AC coupling, both inputs need to be AC coupled irrespective of single-to-differential or differential-to-differential configuration. For higher supply voltages DC coupling of the inputs may be possible provided that the output common mode DC level is set high enough so that the amplifier's inputs and outputs are within their specified operating ranges.

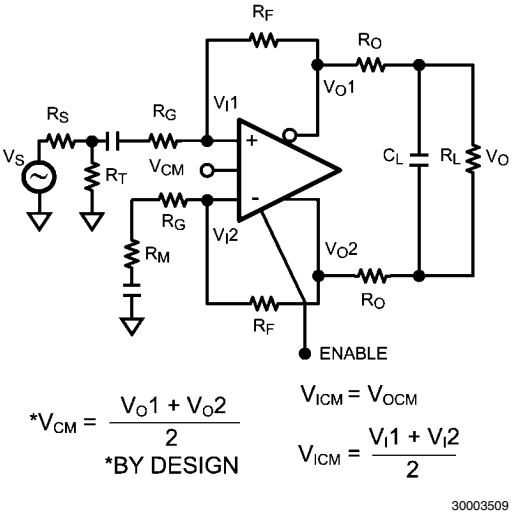


FIGURE 5. AC Coupled for Single Supply Operation

SPLIT SUPPLY OPERATION

For optimum performance, split supply operation is recommended using +5V and −5V supplies; however, operation is possible on split supplies as low as +2.25V and −2.25V and as high as +6V and −6V. Provided the total supply voltage does not exceed the 4.5V to 12V operating specification, non-symmetric supply operation is also possible and in some cases advantageous. For example , if a 5V DC coupled operation is required for low power dissipation but the amplifier input common mode range prevents this operation, it is still possible with split supplies of (V^+) and (V^-). Where (V^+) - (V^-) = 5V and V^+ and V^- are selected to center the amplifier input common mode range to suit the application.

OUTPUT NOISE PERFORMANCE AND MEASUREMENT

Unlike differential amplifiers based on voltage feedback architectures, noise sources internal to the LMH6552 refer to the inputs largely as current sources, hence the low input referred voltage noise and relatively higher input referred current noise. The output noise is therefore more strongly coupled to the value of the feedback resistor and not to the closed loop gain, as would be the case with a voltage feedback differential amplifier. This allows operation of the LMH6552 at much higher gain without incurring a substantial noise performance penalty, simply by choosing a suitable feedback resistor.

Figure 6 shows a circuit configuration used to measure noise figure for the LMH6552 in a 50Ω system. An R_F value of 275Ω is chosen for the SOIC package to minimize output noise while simultaneously allowing both high gain (9 V/V) and proper 50Ω input termination. Refer to the section titled Single Ended Input Operation for calculation of resistor and gain values. Noise figure values at various frequencies are shown in the plot titled Noise Figure in the Typical Performance Characteristics section.

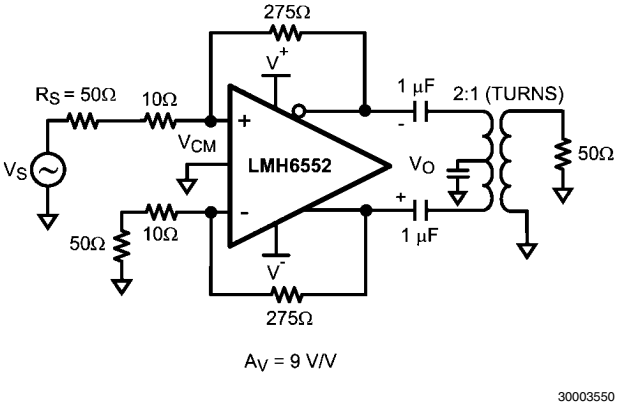


FIGURE 6. Noise Figure Circuit Configuration

DRIVING ANALOG TO DIGITAL CONVERTERS

Analog-to-digital converters present challenging load conditions. They typically have high impedance inputs with large and often variable capacitive components. As well, there are usually current spikes associated with switched capacitor or sample and hold circuits. *Figure 7* shows a combination circuit of the LMH6552 driving the ADC12DL080. The two 125Ω resistors serve to isolate the capacitive loading of the ADC from the amplifier and ensure stability. In addition, the resistors, along with a 2.2 pF capacitor across the outputs (in parallel with the ADC input capacitance), form a low pass anti-aliasing filter with a pole frequency of about 60 MHz. For switched capacitor input ADCs, the input capacitance will vary based on the clock cycle, as the ADC switches between the sample and hold mode. See your particular ADC's datasheet for details.

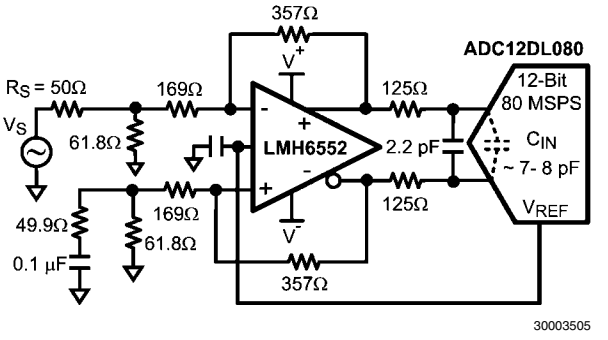


FIGURE 7. Driving a 12-bit ADC

Figure 8 shows the SFDR and SNR performance vs. frequency for the LMH6552 and ADC12DL080 combination circuit with the ADC input signal level at −1 dBFS. The ADC12DL080 is a dual 12-bit ADC with maximum sampling rate of 80 MSPS. The amplifier is configured to provide a gain of 2 V/V in single to differential mode. An external band-pass filter is inserted in series between the input signal source and the amplifier to reduce harmonics and noise from the signal generator. In order to properly match the input impedance seen at the LMH6552 amplifier inputs, R_M is chosen to match $Z_S \parallel R_T$ for proper input balance.

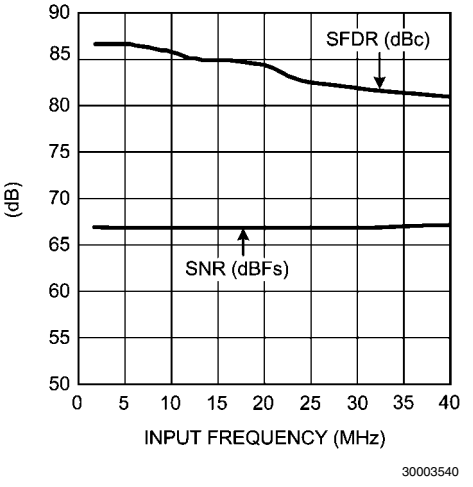


FIGURE 8. LMH6552/ADC12DL080 SFDR and SNR Performance vs. Frequency

Figure 9 shows a combination circuit of the LMH6552 driving the ADC14DS105. The ADC14DS105 is a dual channel 14-bit ADC with a sampling rate of 105 MSPS. The circuit in *Figure 9* has a 2nd order low-pass LC filter formed by the 620 nH inductor along with the 22 pF capacitor across the differential outputs of the LMH6552. The filter has a pole frequency of about 50 MHz. *Figure 10* shows the combined SFDR and SNR performance over frequency with a −1 dBFs input signal and a sampling rate of 1000 MSPS.

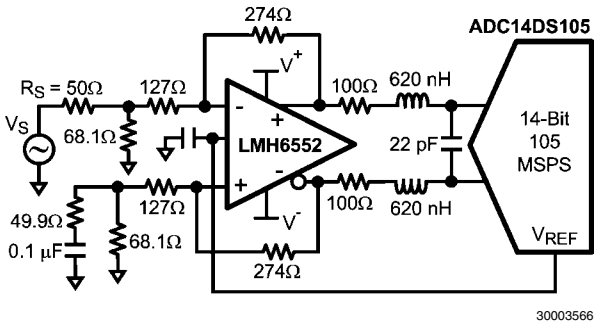


FIGURE 9. Driving a 14-bit ADC

The amplifier is configured to provide a gain of 2 V/V in a single-to-differential mode. The LMH6552 common mode voltage is set by the ADC14DS105. Circuit testing is the same as described for the LMH6552 and ADC12DL080 combination circuit. The 0.1 µF capacitor, in series with the 49.9Ω resistor, is inserted to ground across the 68.1Ω resistor to balance the amplifier inputs.

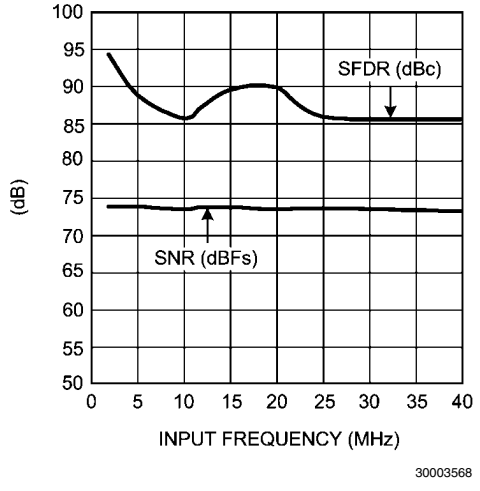


FIGURE 10. LMH6552/ADC14DS105 SFDR and SNR Performance vs. Frequency

The amplifier and ADC should be located as close as possible. Both devices require that the filter components be in close proximity to them. The amplifier needs to have minimal parasitic loading on the output traces and the ADC is sensitive to high frequency noise that may couple in on its input lines. Some high performance ADCs have an input stage that has a bandwidth of several times its sample rate. The sampling process results in all input signals presented to the input stage mixing down into the first Nyquist zone (DC to Fs/2).

The LMH6552 is capable of driving a variety of National Semiconductor Analog-to-Digital Converters. This is shown in Table 3, which offers a list of possible signal path ADC and amplifier combinations. The use of the LMH6552 to drive an ADC is determined by the application and the desired sampling process (Nyquist operation, sub-sampling or over-sampling). See application note AN-236 for more details on the sampling processes and application note AN-1393 'Using High Speed Differential Amplifiers to Drive ADCs. For more information regarding a particular ADC, refer to the particular ADC datasheet for details.

TABLE 3. DIFFERENTIAL INPUT ADC's COMPATIBLE WITH LMH6552 DRIVER

Product Number	Max Sampling Rate (MSPS)	Resolution	Channels
ADC1173	15	8	SINGLE
ADC1175	20	8	SINGLE
ADC08351	42	8	SINGLE
ADC1175-50	50	8	SINGLE
ADC08060	60	8	SINGLE
ADC08L060	60	8	SINGLE
ADC08100	100	8	SINGLE
ADC08200	200	8	SINGLE
ADC08500	500	8	SINGLE
ADC081000	1000	8	SINGLE
ADC08D1000	1000	8	DUAL
ADC10321	20	10	SINGLE
ADC10D020	20	10	DUAL
ADC10030	27	10	SINGLE
ADC10040	40	10	DUAL
ADC10065	65	10	SINGLE
ADC10DL065	65	10	DUAL
ADC10080	80	10	SINGLE
ADC11DL066	66	11	DUAL
ADC11L066	66	11	SINGLE
ADC11C125	125	11	SINGLE
ADC11C170	170	11	SINGLE
ADC12010	10	12	SINGLE
ADC12020	20	12	SINGLE
ADC12040	40	12	SINGLE
ADC12D040	40	12	DUAL
ADC12DL040	40	12	DUAL
ADC12DL065	65	12	DUAL
ADC12DL066	66	12	DUAL
ADC12L063	63	12	SINGLE
ADC12C080	80	12	SINGLE
ADC12DS080	80	12	DUAL
ADC12L080	80	12	SINGLE
ADC12C105	105	12	SINGLE
ADC12DS105	105	12	DUAL
ADC12C170	170	12	SINGLE
ADC14L020	20	14	SINGLE
ADC14L040	40	14	SINGLE
ADC14C080	80	14	SINGLE
ADC14DS080	80	14	DUAL
ADC14C105	105	14	SINGLE
ADC14DS105	105	14	DUAL
ADC14155	155	14	SINGLE

DRIVING CAPACITIVE LOADS

As noted previously, capacitive loads should be isolated from the amplifier output with small valued resistors. This is particularly the case when the load has a resistive component that is 500Ω or higher. A typical ADC has capacitive components of around 10 pF and the resistive component could be 1000Ω or higher. If driving a transmission line, such as 50Ω coaxial or 100Ω twisted pair, using matching resistors will be sufficient to isolate any subsequent capacitance. For other applications see the Suggested R_{OUT} vs. Capacitive Load charts in the Typical Performance Characteristics section.

BALANCED CABLE DRIVER

With up to 15 V_{PP} differential output voltage swing and 80 mA of linear drive current the LMH6552 makes an excellent cable driver as shown in *Figure 11*. The LMH6552 is also suitable for driving differential cables from a single ended source.

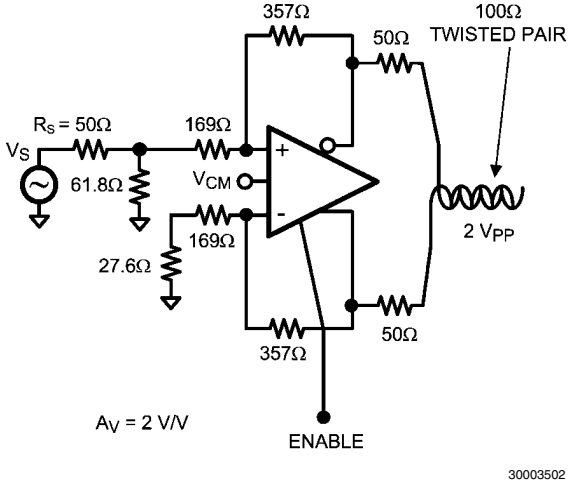


FIGURE 11. Fully Differential Cable Driver

POWER SUPPLY BYPASSING

The LMH6552 requires supply bypassing capacitors as shown in *Figure 12* and *Figure 13*. The 0.01 µF and 0.1 µF capacitors should be leadless SMT ceramic capacitors and should be no more than 3 mm from the supply pins. These capacitors should be star routed with a dedicated ground return plane or trace for best harmonic distortion performance. A small capacitor, ~0.01 µF, placed across the supply rails, and as close to the chip's supply pins as possible, can further improve HD2 performance. Thin traces or small vias will reduce the effectiveness of bypass capacitors. Also shown in both figures is a capacitor from the V_{CM} and ENABLE pins to ground. These inputs are high impedance and can provide a coupling path into the amplifier for external noise sources, possibly resulting in loss of dynamic range, degraded CMRR, degraded balance and higher distortion.

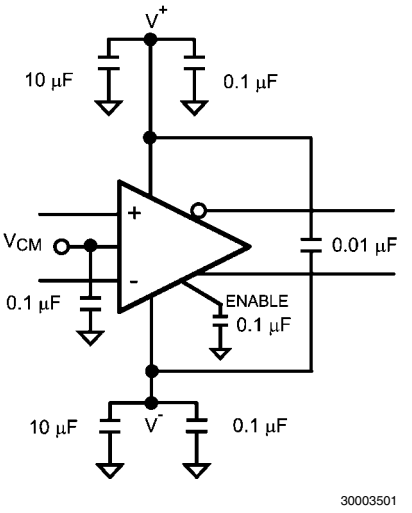


FIGURE 12. Split Supply Bypassing Capacitors

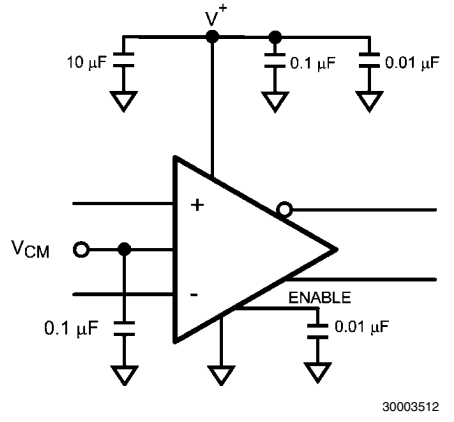


FIGURE 13. Single Supply Bypassing Capacitors

POWER DISSIPATION

The LMH6552 is optimized for maximum speed and performance in the small form factor of the standard SOIC package, and is essentially a dual channel amplifier. To ensure maximum output drive and highest performance, thermal shutdown is not provided. Therefore, it is of utmost importance to make sure that the T_{JMAX} is never exceeded due to the overall power dissipation.

Follow these steps to determine the maximum power dissipation for the LMH6552:

1. Calculate the quiescent (no-load) power: $P_{AMP} = I_{CC}^* (V_S)$, where $V_S = V^+ - V^-$. (Be sure to include any current through the feedback network if V_{OCM} is not mid-rail.)
2. Calculate the RMS power dissipated in each of the output stages: P_D (rms) = rms $((V_S - V^+_{OUT}) * I^+_{OUT})$ + rms $((V_S - V^-_{OUT}) * I^-_{OUT})$, where V_{OUT} and I_{OUT} are the voltage and the current measured at the output pins of the differential amplifier as if they were single ended amplifiers and V_S is the total supply voltage.
3. Calculate the total RMS power: $P_T = P_{AMP} + P_D$.

The maximum power that the LMH6552 package can dissipate at a given temperature can be derived with the following equation:

$P_{MAX} = (150° - T_{AMB})/\theta_{JA}$, where T_{AMB} = Ambient temperature (°C) and θ_{JA} = Thermal resistance, from junction to ambient,

for a given package (°C/W). For the SOIC package θ_{JA} is 150°C/W; LLP package θ_{JA} is 58°C/W.

NOTE: If V_{CM} is not 0V then there will be quiescent current flowing in the feedback network. This current should be included in the thermal calculations and added into the quiescent power dissipation of the amplifier.

ESD PROTECTION

The LMH6552 is protected against electrostatic discharge (ESD) on all pins. The LMH6552 will survive 2000V Human Body model and 200V Machine model events. Under normal operation the ESD diodes have no affect on circuit performance. There are occasions, however, when the ESD diodes will be evident. If the LMH6552 is driven by a large signal while the device is powered down the ESD diodes will conduct . The current that flows through the ESD diodes will either exit the chip through the supply pins or will flow through the device, hence it is possible to power up a chip with a large signal applied to the input pins. Using the shutdown mode is one way to conserve power and still prevent unexpected operation.

BOARD LAYOUT

The LMH6552 is a very high performance amplifier. In order to get maximum benefit from the differential circuit architecture board layout and component selection is very critical. The circuit board should have a low inductance ground plane and well bypassed broad supply lines. External components should be leadless surface mount types. The feedback network and output matching resistors should be composed of short traces and precision resistors (0.1%). The output matching resistors should be placed within 3 or 4 mm of the amplifier as should the supply bypass capacitors. Refer to the section titled Power Supply Bypassing for recommendations on bypass circuit layout. Evaluation boards are available free of charge through the product folder on National's web site.

By design, the LMH6552 is relatively insensitive to parasitic capacitance at its inputs. Nonetheless, ground and power plane metal should be removed from beneath the amplifier and from beneath R_F and R_G for best performance at high frequency.

With any differential signal path, symmetry is very important. Even small amounts of asymmetry can contribute to distortion and balance errors.

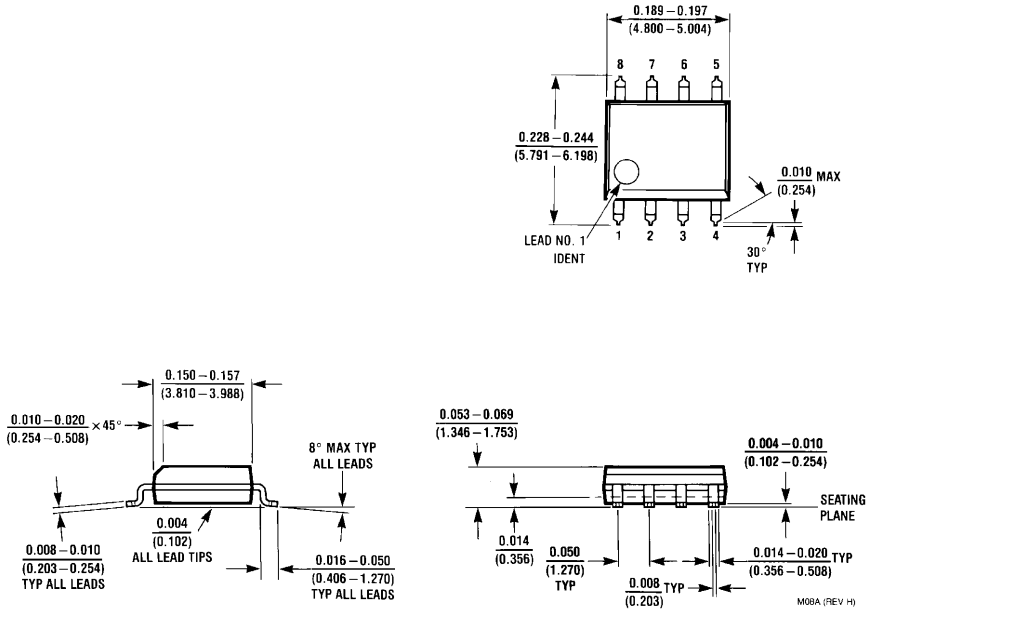
EVALUATION BOARD

National Semiconductor suggests the following evaluation boards to be used with the LMH6552:

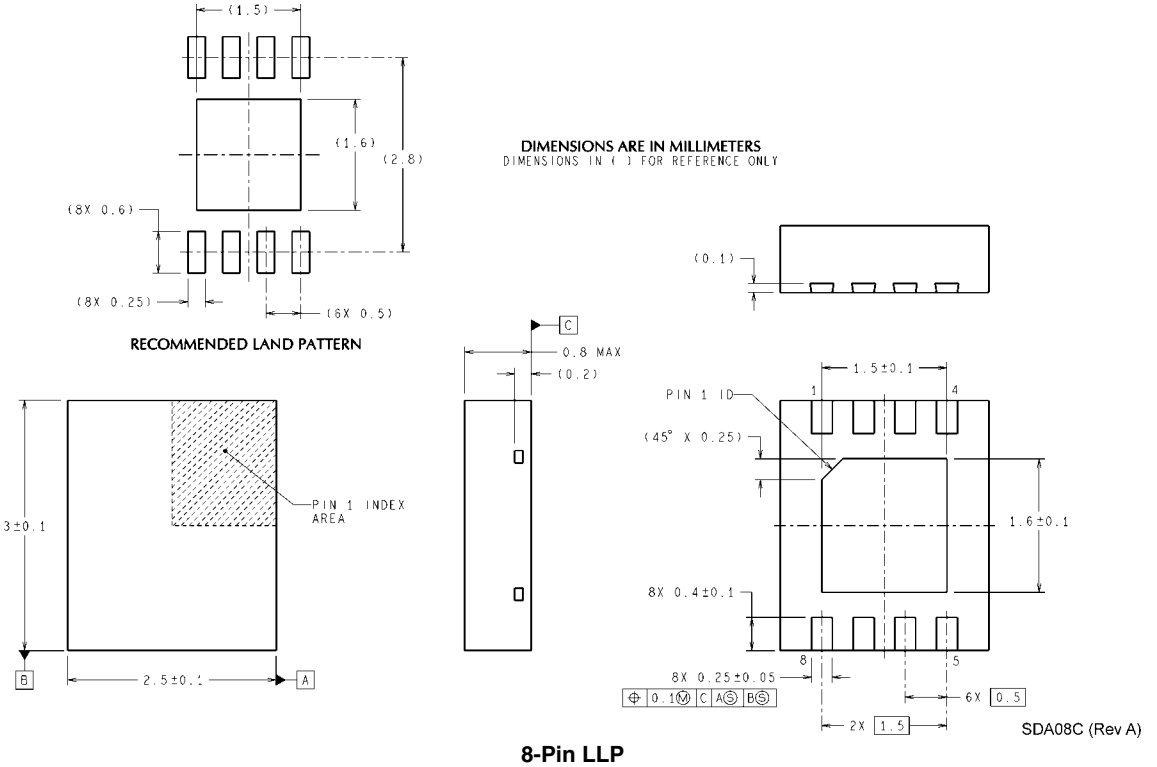
Device	Package	Evaluation Board Ordering ID
LMH6552MA	SOIC	LMH730154
LMH6552SD	LLP	LMH730168

These evaluation boards can be shipped when a device sample request is placed with National Semiconductor.

Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin SOIC
NS Package Number M08A



8-Pin LLP
NS Package Number SDA08C

Notes

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